PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Ehmann et al.	Examiner:	Wilson, Y.
Application No.:	09/955,704	Group Art Unit:	2113
Filed:	September 19, 2001	Docket No.:	US 018159 (VLSI.323PA)
Title:	Data Communication Bus Traffic Generator Arrangement		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Board of Patent Appeals and Interferences, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450, on September 19, 2005.

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APPEAL BRIEF

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Appeal Brief submitted pursuant to 37 C.F.R. § 41.37 for the above-referenced patent application. Please charge Deposit Account No. 50-0996 (VLSI.323PA) in the amount of $500.00 for this brief in support of appeal as indicated in 37 C.F.R. § 41.20(b)(2). If necessary, authority is given to charge/credit deposit account 50-0996 (VLSI.323PA) any additional fees/overages in support of this filing.

I. Real Party in Interest

The real party in interest is the assignee, Koninklijke Philips Electronics, N.V.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-28 are presented for appeal and each of the appealed claims, 1-28, is rejected. The pending claims under appeal may be found in the attached Appendix of Appealed Claims.

IV. Status of Amendments

No amendments were filed subsequent to the final Office Action dated May 3, 2005.

V. Summary of Claimed Subject Matter

The independent claims involved in the appeal are directed to arrangements and methods for generating bus traffic on parallel digital-data paths having multiple traffic sources while increasing availability and minimizing the processing burden on existing bus access resources

One example embodiment of the present invention is directed to a circuit arrangement for generating test-traffic on a digital data path that has at least one other traffic source. *See, e.g.*, FIG. 1 and the corresponding discussion at page 11, line 9 – page 12, line 16. The arrangement includes a data-generation circuit (*e.g.*, 140) adapted to provide a first data stream, a memory arrangement (*e.g.*, 160), state machine circuitry (*e.g.*, 140/150), and a status and feedback circuit (*e.g.*, 170). The memory arrangement is adapted to buffer a plurality of programmable commands, the programmable commands being indicative of at least one of test-traffic: type (*see, e.g.*, page 7, lines 1-12), pattern (*see, e.g.*, page 7, lines 13-25), and behavior-in-time (*see, e.g.*, page 7, line 26 – page 8,

line 6). The state machine circuitry is coupled between the memory arrangement, the data-generation circuit and the digital data path and is adapted to assemble portions of the first data stream into test-traffic where at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands, and is further adapted to generate test-traffic on the digital data path (*e.g.*, 110). The status and feedback circuit is adapted to monitor the digital data path for test-traffic and generate a feedback signal indicative of at least one of test-traffic throughput and test-traffic quality.

Another embodiment of the present invention is directed to a computer system. *See, e.g.*, FIG. 1 and the corresponding discussion at page 11, line 9 – page 12, line 16. The computer system includes a digital data path (*e.g.*, 110); a plurality of traffic sources (*e.g.*, 120, 130, 132, 138); and a circuit arrangement (*see, e.g.*, above paragraph) for generating test-traffic coupled to the digital data path, as described above. Each of the plurality of traffic sources is coupled to the digital data path and adapted to communicate non-test-traffic onto the digital data path and at least one of the plurality of traffic sources is a processor circuit (*e.g.*, 120).

Another embodiment of the present invention is directed to a method of generating test-traffic on a digital data path having at least one other traffic source. *See, e.g.*, FIG. 2 and the corresponding discussion at page 12, line 17 – page 14, line 3. The method includes coupling a dedicated test-traffic source (*e.g.*, 200) to the digital data path (*e.g.*, 210) and providing a first data stream where the first data stream is replicatable. A plurality of programmable commands indicative of at least one type of test-traffic type, pattern and behavior are stored (*e.g.*, 262 and page 17, lines 30-31). Portions of the first data stream are assembled into test-traffic where at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands (*e.g.*, page 13, lines 4-16). The method further includes: generating test-traffic on the digital data path (*e.g.*, page 8, lines 22-27), monitoring the digital data path for the test-traffic, verifying the monitored test-traffic against a corresponding first data stream, and generating a feedback signal indicative of the test-traffic verification (*e.g.*, 272, 274 and page 8, lines 16-21).

Another embodiment is directed to a circuit arrangement for generating test-traffic on a digital data path having at least one other traffic source. *See, e.g.*, FIG. 1 and the

corresponding discussion at page 11, line 9 – page 12, line 16. The arrangement includes means for coupling a dedicated test-traffic source to the digital data path (*e.g.*, interface 180 of FIG. 1 and 32 of FIG. 2) and means for providing a first data stream where the first data stream is replicatable (*e.g.*, traffic generator 100 of FIG. 1 and 200 of FIG. 2). Means for storing (*e.g.*, command memory arrangement discussed at page 6, lines 18-20, 60 of FIG. 1 and 262 of FIG. 2) a plurality of programmable commands that are indicative of at least one type of test-traffic type, pattern and behavior is included. Means for assembling portions of the first data stream into test-traffic (*e.g.*, bus state machine discussed at page 6, lines 20-24, 140/150 of FIG. 1 and 250 of FIG. 2) where at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands is present. The arrangement further includes: means for generating test-traffic on the digital data path (*e.g.*, traffic generator 100 of FIG. 1 and 200 of FIG. 2), means for monitoring the digital data path for the test-traffic (*e.g.*, status and feedback circuit discussed at page 6, line 25-30, 170 of FIG. 1 and 272/274 of FIG. 2), means for verifying the monitored test-traffic against a corresponding first data stream (*e.g.*, status and feedback circuit discussed at page 6, line 25-30, 170 of FIG. 1 and 272/274 of FIG. 2), and means for generating a feedback signal indicative of the test-traffic verification (*e.g.*, status and feedback circuit discussed at page 6, line 25-30, 170 of FIG. 1 and 272/274 of FIG. 2).

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection

A. Claims 1-17, 19-25, 27 and 28 are rejected under 35 U.S.C. § 102(a) over Swanson *et al.* (U.S. Patent No. 6,292,911).

B. Claims 18 and 26 are rejected under 35 U.S.C. § 103(a) over Swanson *et al.* in view of Kim *et al.* (U.S. Patent Publication No. 2002/018678).

VII. Argument

Both grounds of rejection are based on the Examiner's flawed application of the '911 reference to Appellant's claimed invention. The Examiner erroneously attempts to apply the individual test pattern transmission error detection teachings of the '911 reference (*see, e.g.,* Abstract) to Appellant's use of selectable programmable commands for generating different kinds of test traffic and for monitoring a data path for test traffic using a feedback signal. The '911 reference simply teaches a comparison of a sent test pattern with a received test pattern to detect errors in the transmission whereas the claimed invention monitors a data path for test-traffic throughput and quality using test-traffic assembled responsive to programmable commands. A review of the '911 reference reveals no teaching of the claimed programmable commands; state machine circuitry adapted to assemble portions of a first data stream into test-traffic, selected in response to the programmable commands; and a status and feedback circuit. Each of these missing aspects is discussed below.

Without a presentation of correspondence to each of the claimed limitations, neither of the grounds of rejection should be maintained. Appellant accordingly requests that both grounds of rejection be reversed.

A. The rejection of claims 1-17, 19-25, 27 and 28 is improper because the Examiner fails to present correspondence between the cited reference and each of the claimed limitations.

The Examiner fails to present a reference that teaches the claimed programmable commands and therefore also fails to teach a memory arrangement adapted to buffer a plurality of programmable commands. The Examiner erroneously asserts at page 9, that "the programmable commands are the test bit patterns." The '911 test-bit patterns

constitute data that is transmitted from a controller to a storage component whereas the claimed programmable commands influence the portions of the first data stream that are assembled into test-traffic generated on a digital data path. Also, the '911 reference states that the memory 24 merely stores the originally-sent test pattern, which constitutes data. *See, e.g.*, column 4, lines 4-5 and column 6, lines 22-24. Such data fails to correspond to the claimed programmable commands and no further teaching from the '911 reference has been shown to disclose programmable commands, as claimed.

The Examiner also fails to present a reference that teaches the claimed state machine circuitry. The Examiner's reliance on the LFSR 31 of Fig. 2 is misplaced. The '911 reference discloses that the LFSR cycles through a designed sequence and after a complete cycle the LFSR repeats the same sequence, meaning that "the bit pattern sequence being generated is always predictable." *See, e.g.*, column 7, lines 20-24. The '911 reference fails to teach state machine circuitry that is "adapted to assemble portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands."

The Examiner fails to present a reference that teaches a status and feedback circuit, as claimed. The citation to column 7, lines 44-55, discusses a comparison to determine the accuracy of a test pattern received by a component with respect to the test pattern that was generated and transmitted to the component. The received test pattern is transmitted over the channel. No feedback circuit is identified, and no circuit has been identified that is adapted to monitor the digital data path for test-traffic. Moreover, no teachings in the '911 reference have been identified as generating a feedback signal indicative of at least one of test-traffic throughput and test-traffic quality, as claimed.

The '911 reference fails to correspond to the claimed invention with respect to at least these three aspects. Thus, the Examiner's misapplication of the '911 reference fails to provide proper rationale to support the Section 102(a) rejection.

Moreover, several of the instant claim terms are entirely absent from the cited '911 reference. Claim terms such as traffic (or test-traffic), behavior-in-time, throughput, and quality are all absent from the '911 reference. Appellant therefore fails to recognize how the '911 teachings could correspond to Appellant's claimed invention. Further, Appellant fails to recognize any teachings in the '911 reference of programmable

commands that are indicative of specific test-traffic parameters, as discussed at page 7 of the instant Specification. For example, the Specification explains that "traffic pattern" is described as a sequence of traffic generator operations, each operation typically including a direction (*e.g.*, read or write) and an address; and "traffic behavior-in-time" is described as a frequency of generated bus traffic with respect to time. The Examiner does not identify any commands related to data path test-traffic, as claimed and therefore, also does not identify state machine circuitry adapted to assemble portions of the first data stream into test-traffic wherein at least one of type, pattern, and behavior-in-time is selected responsive to the programmable commands, as claimed.

Without a presentation of correspondence to each of the claimed limitations, the rejection is improper and cannot be maintained. Appellant accordingly requests that the rejection be withdrawn.

B. The rejection of dependent claims 18 and 26 is improper for lack of correspondence as addressed above and also because the Examiner fails to present any evidence of motivation to combine the cited references as asserted and fails to overcome the above-argued lack of correspondence between the '911 reference and each of the claimed limitations.

As discussed above in issue A, the Examiner fails to present a reference that teaches each of the claimed limitations. For example, dependent claims 18 and 26 include the above-discussed limitations directed to programmable commands, a memory arrangement adapted to buffer a plurality of programmable commands, state machine circuitry, a status and feedback circuit, and claim terms such as traffic (or test-traffic), behavior-in-time, throughput, and quality. The '911 reference fails to correspond to at least these aspects of the claimed invention, and the Examiner has failed to present evidence to the contrary. Thus, the Examiner's misapplication of the '911 reference fails to provide proper rationale to support the Section 103(a) rejection. Without a presentation of correspondence to each of the claimed limitations, the rejection is improper and cannot be maintained and Appellant accordingly requests that the rejection be withdrawn.

The Examiner acknowledges that the '911 reference fails to teach a digital data path being an AHB protocol bus and fails to present any evidence that the skilled artisan

would be motivated to modify the '911 reference to include an AHB protocol bus. The Examiner's unsupported reasoning for modifying the '911 teachings so that channel 12 is an AHB protocol bus is "because the AHB bus allows the transfer of data from one device to another." Appellant respectfully submits that the '911 channel already allows the transfer of data from one device to another and that any bus, as the term is understood in the electrical arts, would allow the transfer of data from one device to another. The Office Action presents no evidence from the cited references that the skilled artisan would replace the '911 channel 12 with a different type of bus, or more specifically, an AHB protocol bus. Without a presentation of evidence of motivation to modify the cited '911 reference, the Section 103(a) rejection is improper and Appellant requests that it be withdrawn.

The rejection of dependent claims 18 and 26 is also improper for the reasons discussed above in connection with the independent claims. The rejection of claims 18 and 26 relies upon the same primary '911 reference that is shown to be insufficient grounds of rejection as discussed above. "If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious." MPEP § 2143.03; *citing In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). The Examiner has not presented any evidence from the cited references to overcome the above-discussed deficiencies in the '911 teachings. Thus, the rejection of dependent claims 18 and 26 under 35 U.S.C. § 103 should be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections are improper, the claimed invention is patentable, and that the rejections of claims 1-28 should be reversed. Appellant respectfully requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

Should there be any issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Mr. Peter Zawilski, of Philips Corporation at (408) 474-9063.

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APPENDIX OF APPEALED CLAIMS

1. A circuit arrangement for generating test-traffic on a digital data path having at least one other traffic source, comprising:

a data-generation circuit adapted to provide a first data stream;

a memory arrangement adapted to buffer a plurality of programmable commands, the programmable commands indicative of at least one of test-traffic type, pattern and behavior-in-time;

state machine circuitry coupled between the memory arrangement, the data-generation circuit and the digital data path, the state machine circuitry adapted to assemble portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands, and further adapted to generate test-traffic on the digital data path; and

a status and feedback circuit adapted to monitor the digital data path for test-traffic and generate a feedback signal indicative of at least one of test-traffic throughput and test-traffic quality.

2. The circuit arrangement of claim 1, wherein

the state machine circuitry includes a command state machine and a bus master state machine, the command state machine being coupled to the memory arrangement and data-generation circuit, and adapted to direct the bus master state machine to assemble portions of the first data stream into test-traffic having pre-defined type, pattern and behavior-in-time responsive to the programmable commands, and

the bus master state machine is coupled to the digital data path and adapted to communicate the test-traffic onto the digital data path responsive to the command state machine.

3. The circuit arrangement of claim 1, wherein the state machine circuitry is adapted to assemble portions of the first data stream into a test-traffic type selected from a group consisting of 1, 2, 4, 8, 16, 32, and 64 words per burst.

4. The circuit arrangement of claim 1, wherein the state machine circuitry is adapted to assemble portions of the first data stream into a test-traffic type selected from a group consisting of other than 1, 2, 4, 8, 16, 32, and 64 transfers per burst.

5. The circuit arrangement of claim 1, wherein the state machine circuitry is further adapted to receive the first data stream from the data-generation circuit without generating test-traffic on the digital data path.

6. The circuit arrangement of claim 1, wherein the state machine circuitry is adapted to pause in response to programmable commands.

7. The circuit arrangement of claim 1, further comprising a bus interface circuit coupled between the memory arrangement and the digital data path, the bus interface circuit adapted to pass programmable commands received via the digital data path to the memory arrangement.

8. The circuit arrangement of claim 1, wherein the first data stream is a repeatable sequence of binary data.

9. The circuit arrangement of claim 8, wherein the data-generation circuit is a second memory arrangement, the first data stream being stored in the second memory arrangement.

10. The circuit arrangement of claim 8, wherein the first data stream comprises a sequence of pseudo-random numbers.

11. The circuit arrangement of claim 10, wherein the data-generation circuit is a second memory arrangement, the first data stream being stored in the second memory arrangement.

12. The circuit arrangement of claim 10, wherein the data-generation circuit is a linear feedback shift register (LFSR) circuit, the first data stream comprising a sequence of LFSR values.

13. The circuit arrangement of claim 12, wherein the state machine circuitry is configured and arranged to seed the LFSR and control content of the first data stream.

14. The circuit arrangement of claim 13, wherein the status and feedback circuit is further adapted to verify monitored test-traffic against corresponding LFSR values, and the feedback signal being an interrupt generated indicative of the test-traffic verification.

15. The circuit arrangement of claim 1, wherein the status and feedback circuit is further adapted to verify monitored test-traffic against a corresponding first data stream, and the feedback signal being an interrupt generated indicative of the test-traffic verification.

16. The circuit arrangement of claim 15, wherein the memory arrangement includes command registers adapted to store programmable commands, configuration registers adapted to store traffic generation process control information and status registers adapted to store test-traffic verification information.

17. The circuit arrangement of claim 1, wherein the status and feedback circuit includes a counter adapted to specify a number of command repetitions, and a loop timer adapted to specify a period within which a set of programmable commands must execute.

18. The circuit arrangement of claim 1, wherein the digital data path is an AHB protocol bus.

19. A computer system, comprising:

a digital data path;

a plurality of traffic sources, each traffic source coupled to the digital data path and adapted to communicate non-test-traffic onto the digital data path; and

a circuit arrangement for generating test-traffic coupled to the digital data path, the circuit arrangement including,

a data-generation circuit adapted to provide a first data stream,

a memory arrangement adapted to buffer a plurality of programmable commands, the programmable commands indicative of at least one of test-traffic type, pattern and behavior;

state machine circuitry coupled between the memory arrangement, the data-generation circuit and the digital data path, the state machine circuitry adapted to assemble portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands, and further adapted to generate test-traffic on the digital data path; and

a status and feedback circuit adapted to monitor the digital data path for test-traffic and generate a feedback signal indicative of at least one of test-traffic throughput and test-traffic quality, wherein at least one of the plurality of traffic sources is a processor circuit.

20. The circuit arrangement of claim 19, wherein the data-generation circuit is a linear feedback shift register (LFSR) circuit, the first data stream consists of a sequence of pseudo-randomly generated binary numbers representing LFSR values.

21. The circuit arrangement of claim 20, wherein the status and feedback circuit is further adapted to verify monitored test-traffic against a corresponding first data stream, and the feedback signal is an interrupt generated indicative of the test-traffic verification.

22. A method of generating test-traffic on a digital data path having at least one other traffic source, comprising:

coupling a dedicated test-traffic source to the digital data path;

providing a first data stream, the first data stream being replicatable;

storing a plurality of programmable commands, the programmable commands indicative of at least one of test-traffic type, pattern and behavior;

assembling portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands;

generating test-traffic on the digital data path;

monitoring the digital data path for the test-traffic;

verifying the monitored test-traffic against a corresponding first data stream; and

generating a feedback signal indicative of the test-traffic verification.

23. The method of claim 22, wherein the first data stream is a sequence of pseudo-random numbers each representative of a linear feedback shift register (LFSR) value.

24. The method of claim 23, further comprising, verifying monitored test-traffic against a corresponding LFSR value, wherein the feedback signal is an interrupt indicative of each test-traffic verification.

25. The method of claim 22, further comprising:

counting a pre-determined number of command-execution repetitions;

timing each command-execution repetition against an associated programmable period; and

generating a feedback signal indicative a command-execution repetition exceeding the associated programmable period.

26. The method of claim 22, wherein the digital data path is an AHB protocol bus.

27. The method of claim 26, wherein
test-traffic type is one of a group consisting of 1, 2, 4, 8, 16, 32, and 64 transfers per burst.

28. A circuit arrangement for generating test-traffic on a digital data path having at least one other traffic source, comprising:

means for coupling a dedicated test-traffic source to the digital data path;

means for providing a first data stream, the first data stream being replicatable;

means for storing a plurality of programmable commands, the programmable commands indicative of at least one of test-traffic type, pattern and behavior;

means for assembling portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands;

means for generating test-traffic on the digital data path;

means for monitoring the digital data path for the test-traffic;

means for verifying the monitored test-traffic against a corresponding first data stream; and

means for generating a feedback signal indicative of the test-traffic verification.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.